

FIG.1

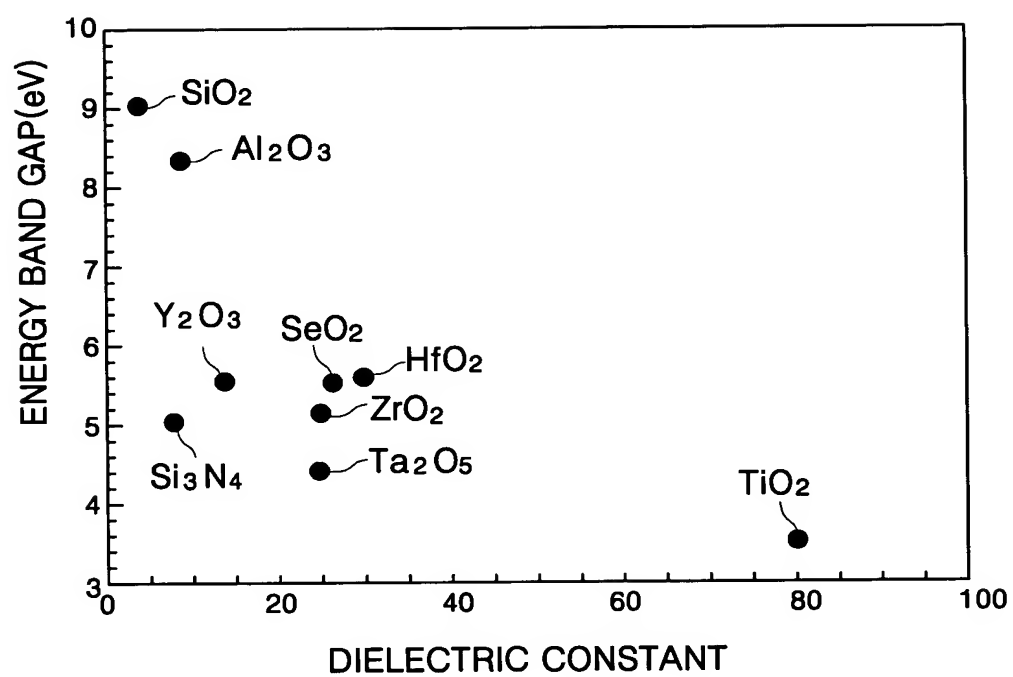


FIG.2A

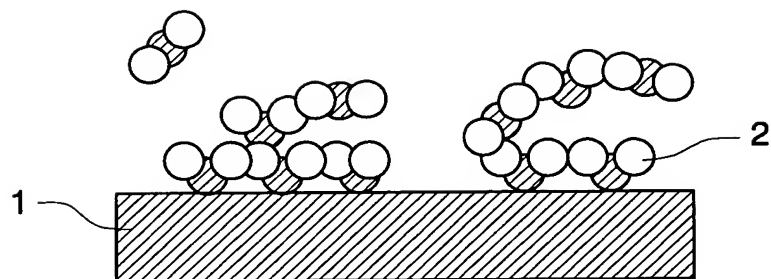


FIG.2B

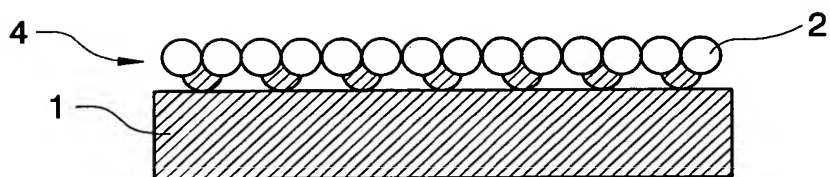


FIG.2C

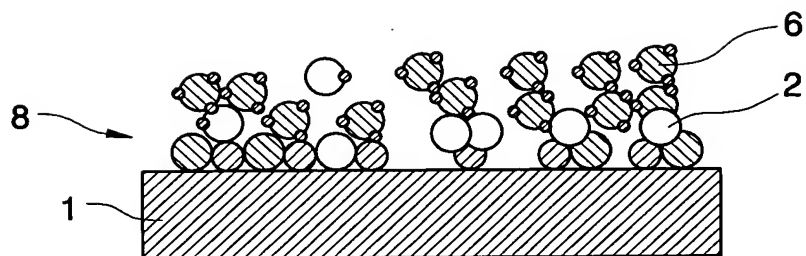


FIG.2D

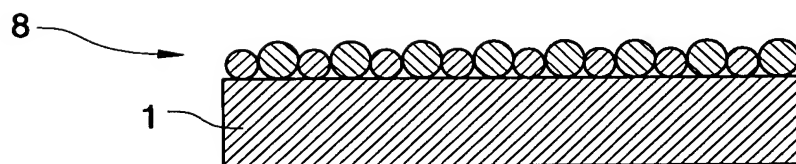


FIG.2E

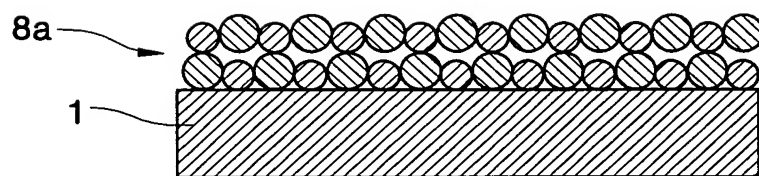


FIG.3

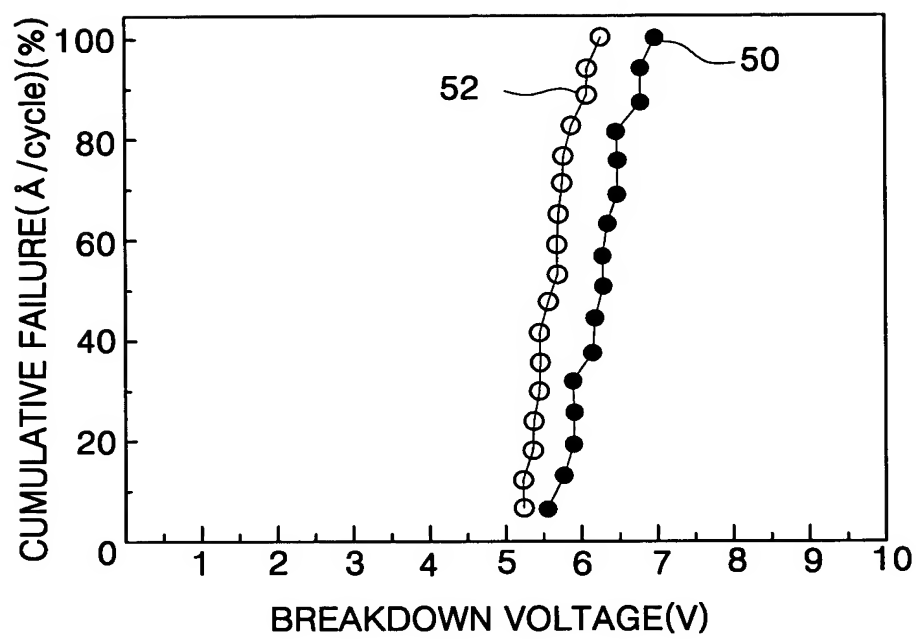


FIG.4A

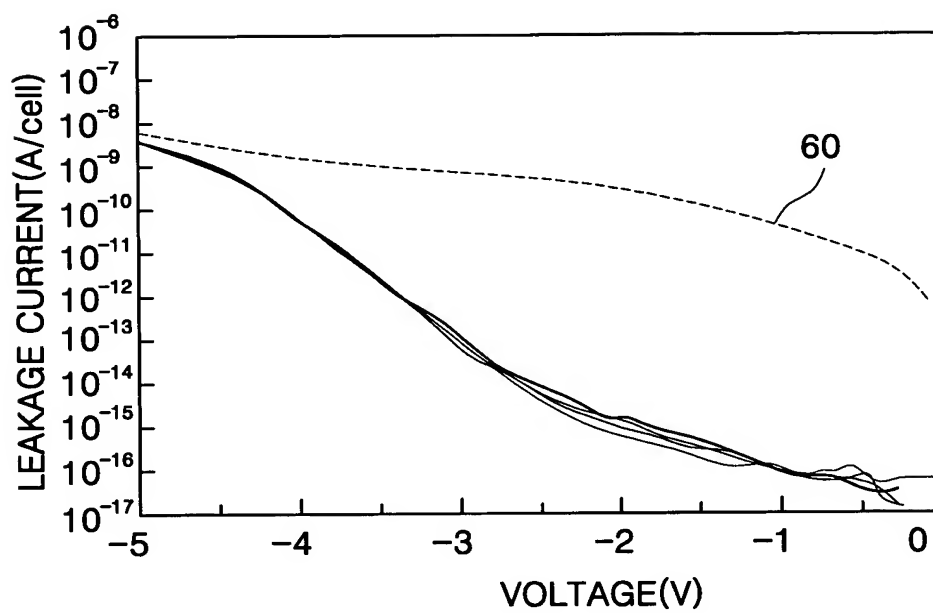


FIG.4B

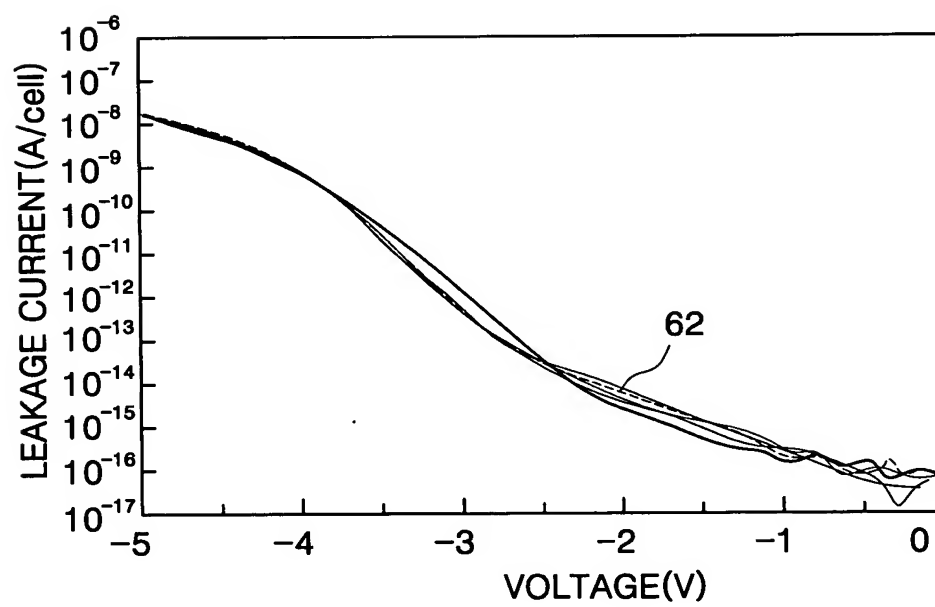


FIG.5

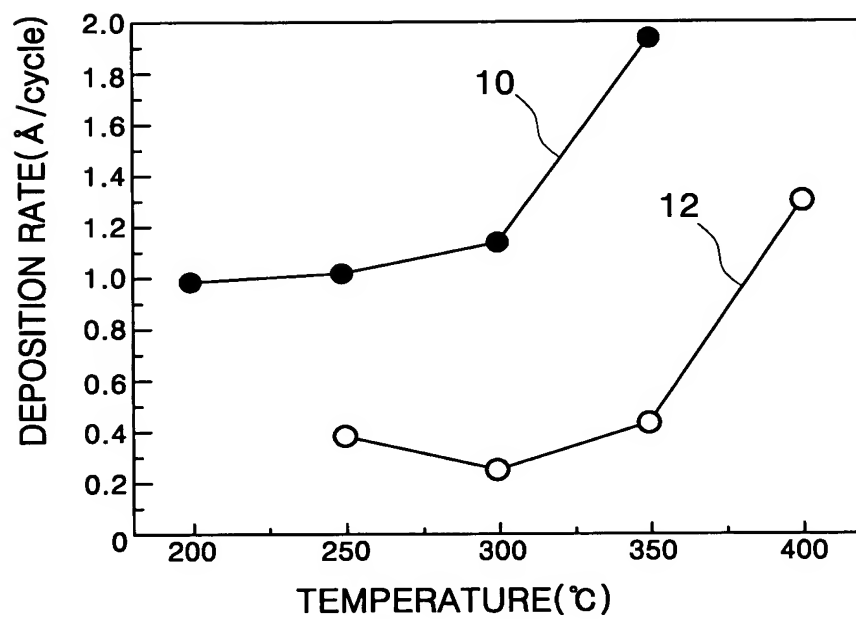


FIG.6

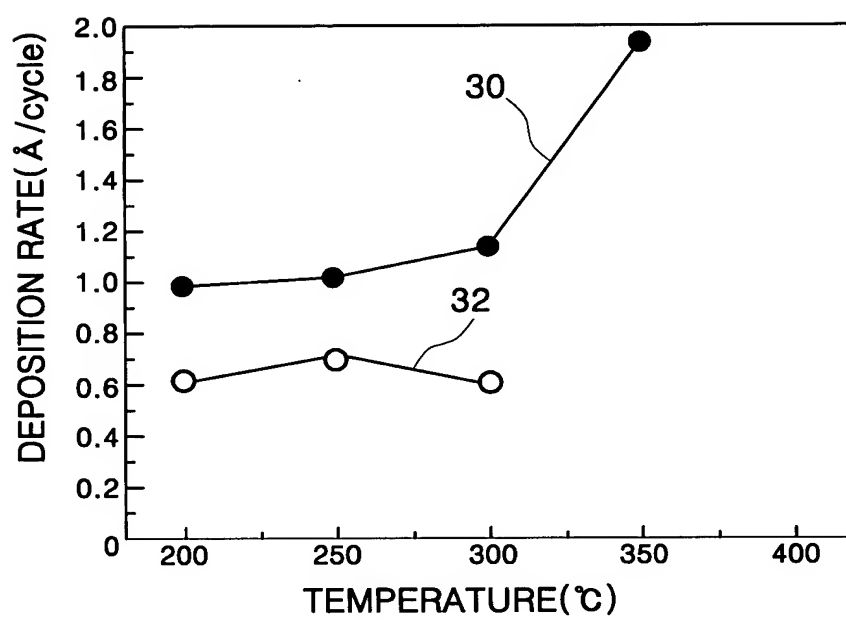




FIG.7

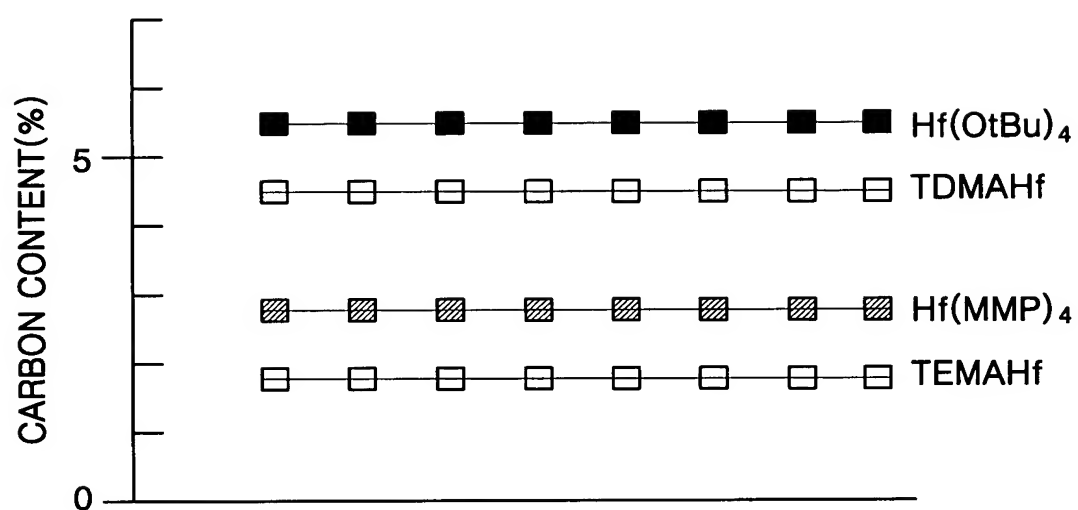


FIG.8A

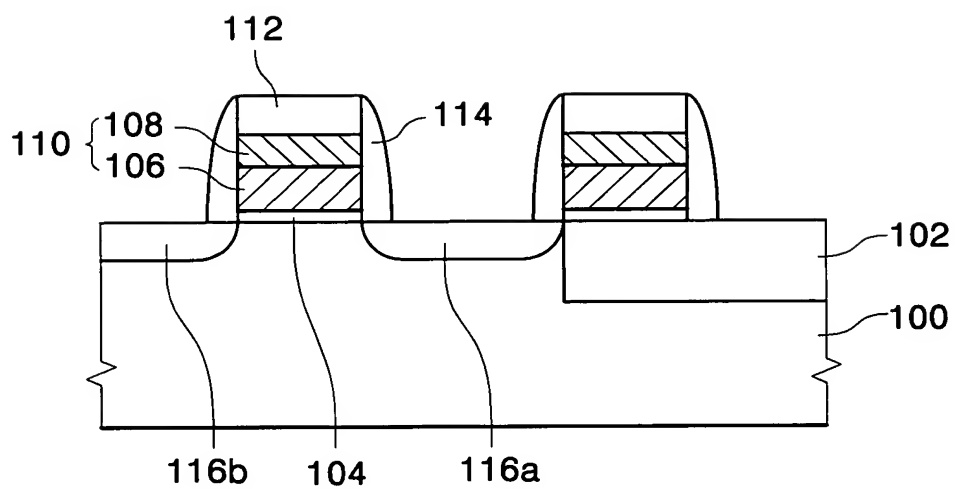


FIG.8B

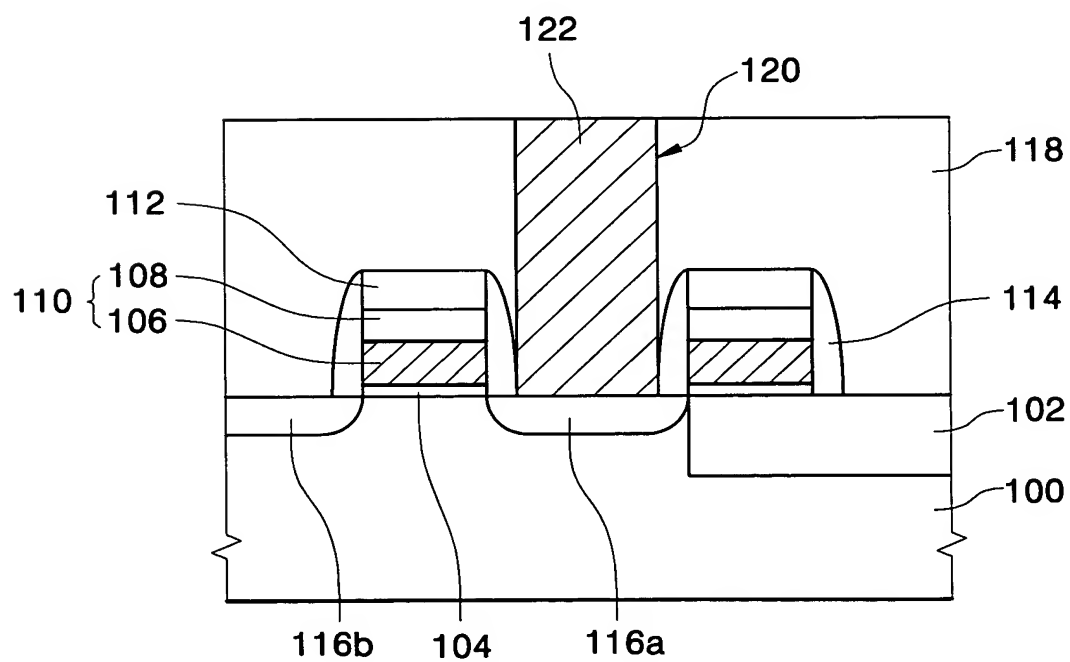
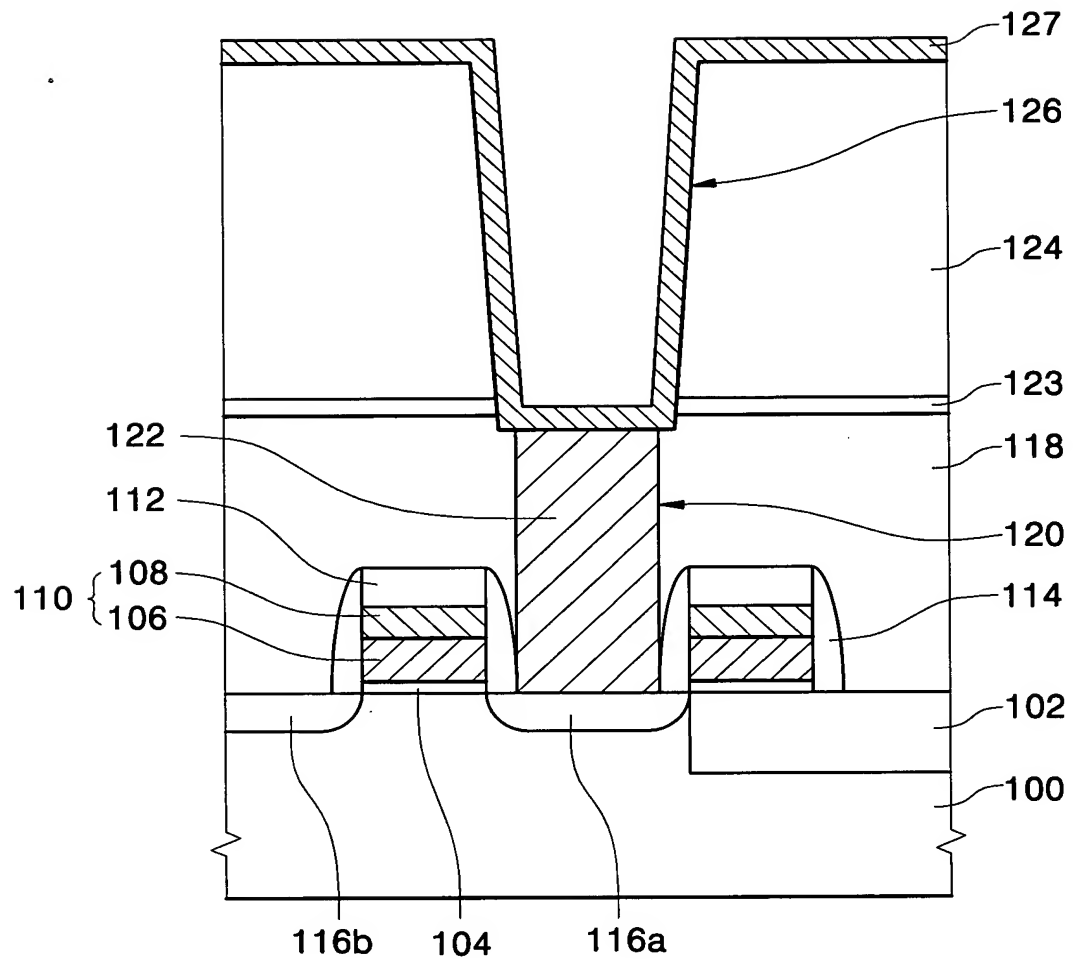


FIG.8C



This cross-sectional view shows a central gate structure 120 with a gate dielectric 122 and a gate electrode 128. The gate structure is flanked by side gates 110, each consisting of a gate dielectric 108 and a gate electrode 106. The device is built on a substrate 100 with a base layer 102. A layer 118 is located above the gate structure. The thickness of the gate dielectric 122 is indicated as  $t_1$ , and the thickness of the gate electrode 128 is indicated as  $t_2$ . The regions 116a and 116b are shown at the bottom of the device, and 104 is the region between the side gates.

This cross-sectional view shows a central gate structure (120) with a gate stack (112, 122) and a gate body (114). The gate is flanked by side spacers (116a, 116b) and a central spacer (104). The device is built on a substrate (100) with a base layer (102). The side spacers (116a, 116b) are composed of layers 106 and 108. The central spacer (104) is composed of layers 110 and 112. The gate stack (112, 122) is composed of layers 120 and 123. The gate body (114) is composed of layers 128, 130, and 132. The side spacers (116a, 116b) are also composed of layers 128, 130, and 132. The central spacer (104) is composed of layers 128, 130, and 132. The gate stack (112, 122) is composed of layers 120 and 123. The gate body (114) is composed of layers 128, 130, and 132. The side spacers (116a, 116b) are also composed of layers 128, 130, and 132.

FIG.9

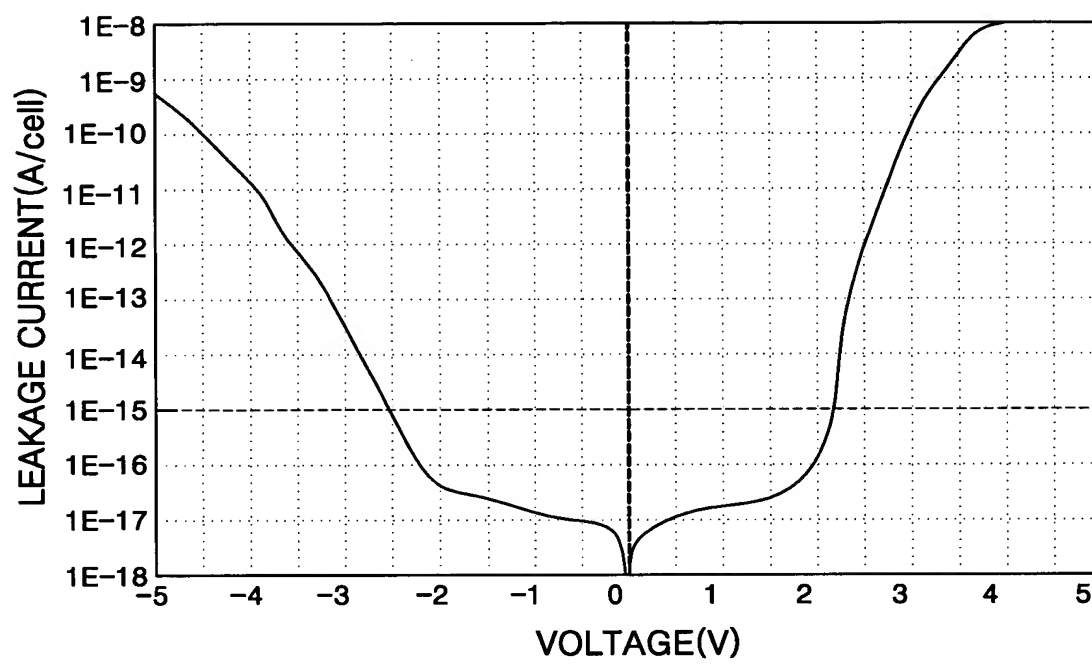


FIG.10

